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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/525,597	02/25/2005	Nevio Benvenuto	IT02 0025 US	3611

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EXAMINER	
NEFF, MICHAEL R	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
04/03/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/525,597	BENVENUTO ET AL.	
	Examiner	Art Unit	
	MICHAEL R. NEFF	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,17-28 and 33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,17-28 and 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

2. Applicant's arguments with respect to claims 1-33 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claims 6 and 23 objected to because of the following informalities: Both claims contain the term 'signal to parallel' which the examiner believes is intended to read 'serial to paralllel'. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1-10, 12, 18-27 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Birru (US Publication 2002/0037058 A1) in view of Raghavan (US Patent 6,115,418).

Re claims 33, 1 and 18, Birru discloses a frequency-domain decision feedback equalizer device and associated method for single carrier modulation, the device comprising:

a first section including a fast Fourier transformer (Figure 12, element 1103) to perform a fast Fourier transformation on a first vector of single carrier signals inputted into said first section (Paragraph 0005-0007, 0024 which while directed at figure 2 explains the FFT system function in greater detail), and to output the transformed signals as a second vector of signals (output of 1103; paragraph 0024),

a feed forward equalizer (1104) to perform a feed forward equalization by generating equalization parameters using a fast Fourier transformation (1207) estimation of a channel impulse response (output of 1206; paragraphs 0007) of an output single carrier signal (Paragraph 0005) of said first section, multiplying each of the components of said second vector of signals with the generated equalization parameters (Figure 12, elements 1105 and output from 1104) to reduce the signal-noise ratio of the signals (Paragraphs 0054-0055; Figure 6), and outputting the multiplied signals as a third vector of signals (output of 1105; Paragraph 0025), and

an inverse fast Fourier transformer to perform an inverse fast Fourier transformation on said third vector of signals (Figure 12, element 1106), and to output the inversely transformed signals as a fourth vector of signals that is the output signal of the first section (output of 1106; paragraphs 0038, 0005-0007) however Birru fails to explicitly disclose a second section including a feedback filter to linearly filter a signal derived from an output signal of said second section, an adder to add the output signal of said feedback filter to the output signal of said first section, and a detector to receive the output signal of said adder and generate said output signal of said second section by extracting samples from the output signal of said adder.

These designs are however disclosed by Raghavan. Raghavan discloses a decision feedback equalizer comprising a feedback filter (Figure 7, element 429) to linearly filter a signal derived from an output signal of said second section (Figure 7, element 408), an adder (Figure 7, element 421) to add the output signal of said feedback filter (output of 429 which is input to 421) to the output signal of said first section (input signal yk to element 421), and a detector (Figure 7, element 404) to receive the output signal of said adder and generate said output signal of said second section by extracting samples from the output signal of said adder (output of 404; Col. 10 line 13-Col. 11 line 3 provide detailed disclosure of the DFE design).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the frequency-domain equalizer design as disclosed by Birru to incorporate the decision feedback equalizer design as disclosed by Raghavan in order to incorporate the recursive and well known design into the aspect of the sample discarding/selection after the forward equalization takes place in first section of the design allowing for the added benefit of utilizing feedback decision elements to dynamically reduce the ISI effects within the system as explained by Raghavan.

Re Claims 2 and 19, the combined disclosure of Birru and Raghavan as a whole disclose the device according to claims 1 and 18, Birru further discloses wherein said feed forward equalization means is provided for generating equalization parameters adapted for minimizing the signal-to-noise ratio of the signal processed in the frequency-domain decision feedback equalizer device, preferably in the output signal of

said first section (Figure 12, elements 1105 and output from 1104; Paragraphs 0054-0055; Figure 6).

Re Claims 3 and 20, the combined disclosure of Birru and Raghavan as a whole disclose the device according to claims 1 and 18, Birru further discloses wherein said feed forward equalization means is provided for generating equalization parameters by taking into account a fast Fourier transformation (1207) estimation of a channel impulse response (output of 1206) of the signal processed in the frequency-domain decision feedback equalizer device, preferably in the output signal of said first section (Figure 12, elements 1104, 1207, output of 1206; paragraphs 0007).

Re Claims 4 and 21, the combined disclosure of Birru and Raghavan as a whole disclose the device according to claims 1 and 18, Birru further discloses wherein said first section further comprises: a serial to parallel converting means for converting a sequence of signals inputted into said first section to said first vector of signals (1102), and a parallel to serial converting means for converting said fourth vector of signals to a sequence of output signals of said first section (1107).

Re Claims 5 and 22, the combined disclosure of Birru and Raghavan as a whole disclose the device according to claims 4 and 21, Birru further discloses wherein said serial to parallel converting means is adapted to receive scalar signals (Paragraph 0005 symbol stream input to S/P).

Re Claims 6 and 23, the combined disclosure of Birru and Raghavan as a whole disclose the device according to claims 4 and 21, Birru further discloses wherein said signal to parallel converting means is provided to generate said first vector of signals including blocks of a predetermined number of consecutive samples of the signals inputted into said first section (Paragraph 0005-0006; M, N size elements).

Re Claims 7 and 24, the combined disclosure of Birru and Raghavan as a whole disclose the device according to claims 4 and 21, Birru further discloses wherein said parallel to serial converting means and said feedback filter means are provided to output scalar signals (Paragraph 0005-0007).

Re Claims 8 and 25, the combined disclosure of Birru and Raghavan as a whole disclose the device according to claims 6 and 23, Birru further discloses wherein said parallel to serial converting means is provided to output a scalar signal which is constituted by consecutive blocks of a predetermined number of samples, each block being built with the predetermined number of samples of each block of said fourth vector of signals (Paragraphs 0005-0007 M and N elements).

Re Claims 9 and 26, the combined disclosure of Birru and Raghavan as a whole disclose the device according to claims 1 and 18, Raghavan further discloses wherein

said detector means is adapted to receive and output discrete time signals (Col. 3 lines 23-24; equations 2 and 3 shows sample time is relevant in detection means).

Re Claims 10 and 27, the combined disclosure of Birru and Raghavan as a whole disclose the device according to claims 1 and 18, Raghavan further discloses wherein said detector means is provided to generate said output signal (404, output from 404).

Re Claim 12, the combined disclosure of Birru and Raghavan as a whole disclose the device according to claim 1, Birru further discloses wherein a receiver of a communication system using a single carrier modulation (paragraph 0005), wherein said receiver includes said first and second sections of the frequency-domain decision feedback equalizer device (combination of cited disclosure as applied above wherein Birru represents the 'first section' and Raghavan represents the 'second section').

6. **Claims 11 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Birru and Raghavan as applied to claim 1 and 18 above, and further in view of Johnson et al. (herein after Johnson) (US Patent 5,808,574).**

Re Claims 11 and 28, the combined disclosure of Birru and Raghavan as a whole disclose the device according to claims 1 and 18; Raghavan further discloses wherein said second section further comprises a feedback input generator means for receiving said output signal of said second section and providing an output signal which

is built by consecutive blocks, each block comprising a predetermined number (M) of samples from said output signal of said section, to said feedback filter means (Col. 10 lines 25-62); however the combination of Birru and Raghavan fails to explicitly disclose wherein each block is also including a pseudo noise sequence.

This design is however disclosed by Johnson. Johnson discloses a feedback system within a communication system wherein the signals within the feedback loop are adjusted to include a pseudo noise sequence (Col. 45 lines 29-43).

Therefore it would have been obvious to one of ordinary skill in the art a the time the invention was made to modify the feedback equalizer disclosure of Birru and Raghavan to insert pseudo noise into the feedback signal as disclosed by Johnson in order to gain the benefit of improving on system performance and symbol detection.

7. **Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Birru and Raghavan as applied in claim 1, and further in view of Thomas et al. (herein after Thomas) (US Publication 2004/0013084 A1).**

Re Claim 17, the combined disclosure of Birru and Raghavan as a whole disclose the device according to claim 1; Birru further discloses a communication system including a transmitter using a single carrier modulation (Paragraphs 0005, 0022-0023), for transmitting data, comprising a modulating means for organizing the data in blocks wherein each block is separated by a sequence of a predetermined signal (Paragraphs 0005, 0022-0023; inherent aspects of the transmit/receive capacity of the disclosed system) and a receiver of a communication system using a single

carrier modulation (Paragraph 0005), wherein said receiver includes said first and second sections of the frequency-domain decision feedback equalizer device (combination of cited disclosure as applied above wherein Birru represents the 'first section' and Raghavan represents the 'second section'), however the combination fails to explicitly disclose wherein each block is separated by a sequence of a predetermined signal.

However these limitations are explicitly disclosed by Thomas. Thomas discloses separating each data block by a sequence of a predetermined signal, or a signal header, is explicitly disclosed by Thomas (Fig. 1-5).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate separating the data symbol blocks by a predetermined header symbol as disclosed by Thomas with the feedback equalizer as disclosed by Berberidis in order to gain the benefit of improved symbol recognition and demodulating within the receiver end of the communication system.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL R. NEFF whose telephone number is (571)270-1848. The examiner can normally be reached on Monday - Friday 8:00am - 4:30pm EST ALT Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on (571)272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MICHAEL R. NEFF/
Examiner, Art Unit 2611

/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611